Purpose

This document provides an overview of recommended SMT process guidelines for PolyStrata surface mount components. Note that these are intended only as guidelines and not a mandatory ruleset. Designers should always work in tandem with the final assembler/manufacturer to ensure a robust SMT process.

Stencil Design

To ensure proper paste is applied to the PCB, the correct stencil sizing must be used. IPC-7525C outlines stencil design guidelines and should always be followed for a repeatable manufacturing process. Two important parameters to consider are the stencil thickness and coating.

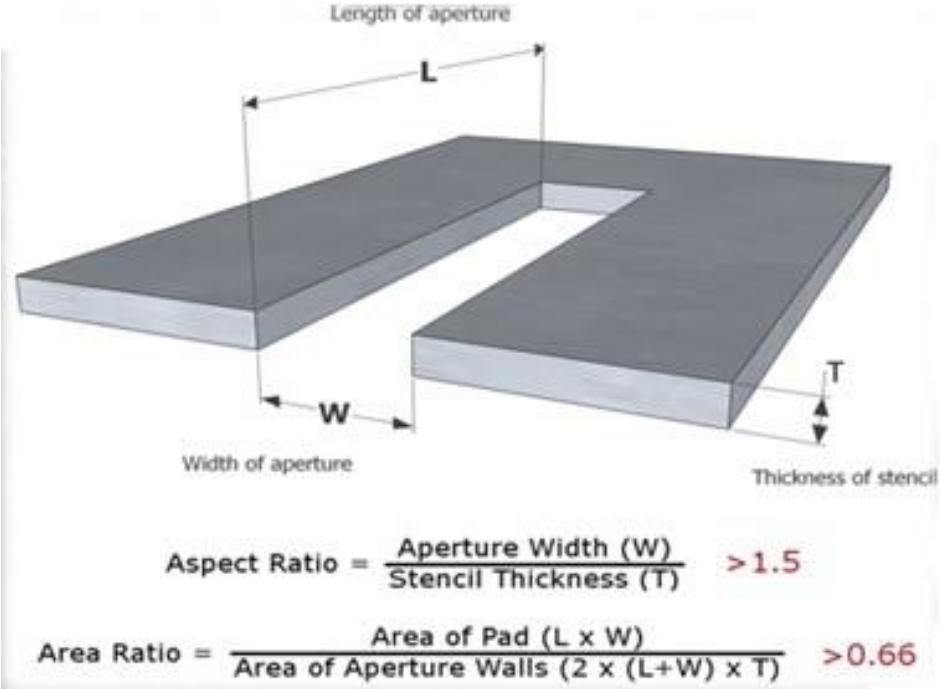


Figure 1 - IPC Stencil Sizing Guidelines

The calculation outlined in Figure 1 is critical for repeatable solderability. Aspect and area ratios should be kept to at least 1.5 and 0.66 respectively. This will ensure proper release of the solder paste release from the stencil without under pasting the part.

Example Calculation

Below is an example calculation of the stencil thickness using the recommended paste pattern from a PolyStrata RF launch:

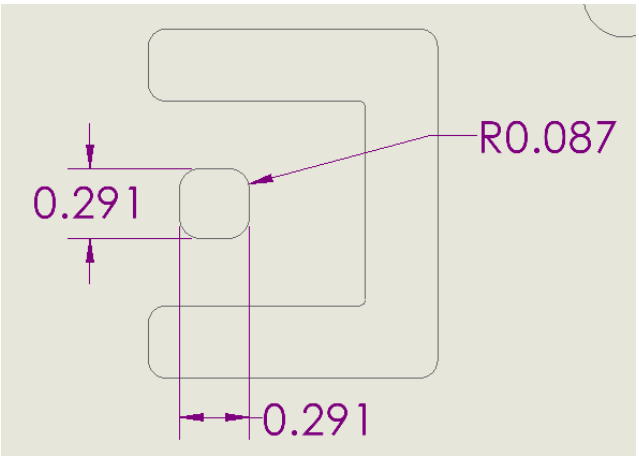


Figure 2 - Launch Pin Geometry

$$Aspect\ Ratio\ = \frac{Width}{Thickness} > 1.5$$

$$\frac{0.291mm}{T} > 1.5 \rightarrow \boldsymbol{T < 0.194mm}$$

Now that we have a thickness of 0.194mm (7.6mil) from the above equation, we need to compare to the minimum area ratio:

$$Area\ Ratio\ = \frac{Area\ of\ Pad\ (L * W)}{Area\ of\ Walls\ (2 * (L + W) * T)} > 0.66$$

$$Area\ Ratio\ = \frac{0.085mm^2}{2 * 0.582mm * T} > 0.66 \rightarrow \boldsymbol{T < 0.110mm}$$

From the two above equations, we find that the stencil thickness must be less than 0.194mm (7.6mil) to not violate the aspect ratio, and less than 0.110mm (4.3mil) to not violate the area ratio. Therefore, the stencil must be less than 4.3mil thick for the final design.

Paste Type

In addition to stencil thickness, the correct paste type should be used for good stencil release. IPC guidelines recommend the “five-ball rule”, meaning that the solder paste ball size should allow for five solder balls to fit in the minimum aperture window.

Type	Less than 0.5% larger than	10% Max. between	80% Min. Between	10% Max. Less than
1	160	150-160	75-150	75
2	80	75-80	45-75	45
3	60	45-60	25-45	25
4	50	38-50	20-38	20
5	40	25-40	15-25	15
6	25	15-25	5-15	5
7	15	11-15	2-11	2

Figure 3 - Solder Paste Size by Type (microns)

Figure 3 shows the solder paste type definition by ball size (units are in microns). Using our example RF pin launch, the minimum aperture size is 0.291mm:

$$\frac{291um}{5\ solder\ balls} = 58um$$

Using the five-ball rule from the equation above, we see that Type 4 paste meets the 58um maximum ball size for the 0.5% case. Using the worst-case value from the 0.5% column ensures maximum repeatability of the paste release during high-volume production.

Reflow Profiles

PolyStrata SMT components are compatible with standard leaded and non-leaded reflow profiles. The choice of reflow profile should be dictated by the recommended reflow from the solder paste vendor. An example generic profile provided by Kester for their leaded and lead-free solder pastes is shown below:

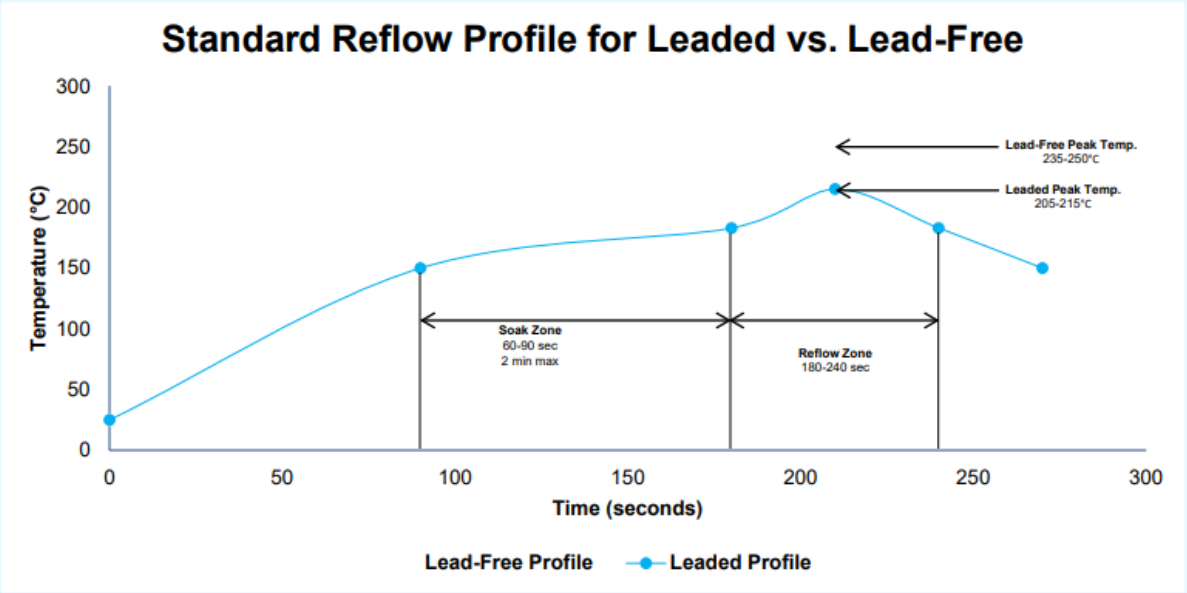


Figure 4 - Reflow Profiles from Kester

Always follow recommended profiles for proper wetting of the PolyStrata RF launches during assembly.

Pick and Place

All PolyStrata SMT components are compatible with standard pick and place assembly processes. It's recommended to follow these precautions for proper placement:

1. Keep fiducial references as close to the PolyStrata component as possible. The accuracy of the pick and place head is affected by distanced traversed from the fiducial reference. By placing a fiducial reference close to the component, this error can be minimized.
2. Reduce the head speed during placement. With high head speeds, parts can slide along the vacuum head of the pick and place due to abrupt changes in speed as the head starts and stops. This creates a translation error between the pickup and place point on the PCB. Reducing the head speed will reduce these errors.
3. Use copper alignment features instead of silkscreen. Generally speaking, the solder mask and copper alignment are much more accurate than silkscreen. Therefore, it can be beneficial to use copper alignment features on the board for optical inspection. An example is shown below in Figure 5.

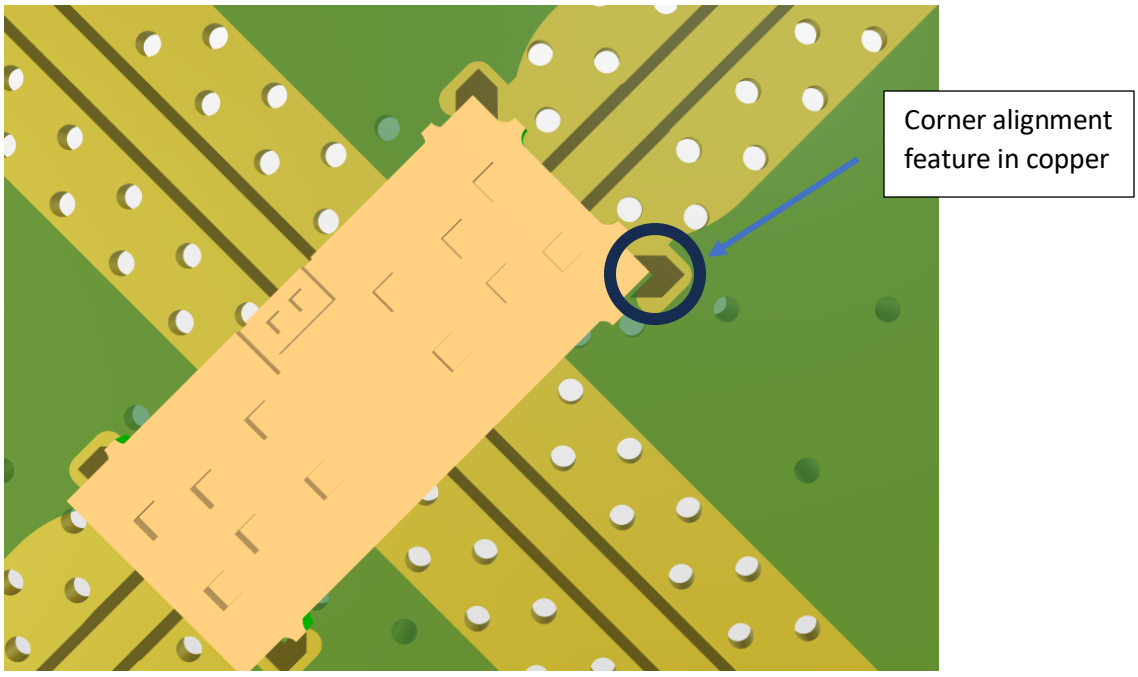


Figure 5 - Copper Alignment PCB Feature

4. Use proper pickup location and size for the component (outlined in the interface control drawing):

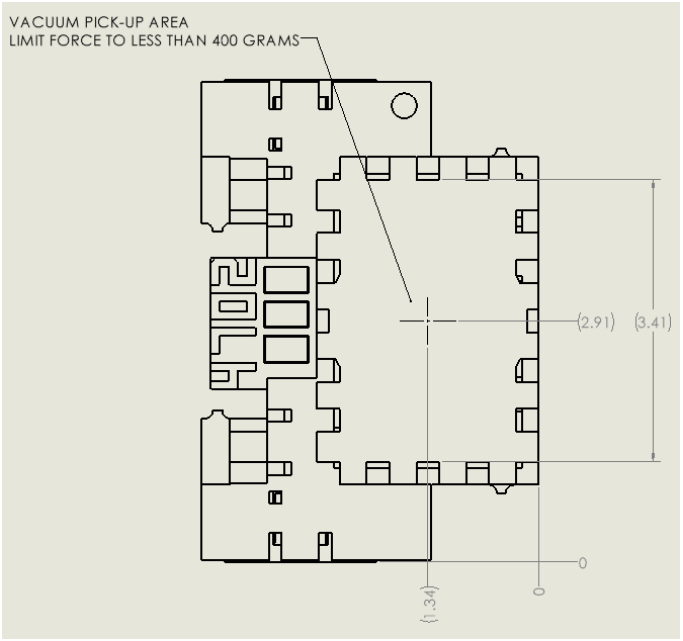


Figure 6 - Vacuum Pickup Area

Footprint

Part footprints are available in DXF and native Altium Designer formats on request. Please reach out to your Nuvotronics representative to receive these files. Alternatively, a footprint can be made from the mechanical model of the PolyStrata part. Please follow the below guidelines for layer expansion when creating a footprint for PolyStrata components:

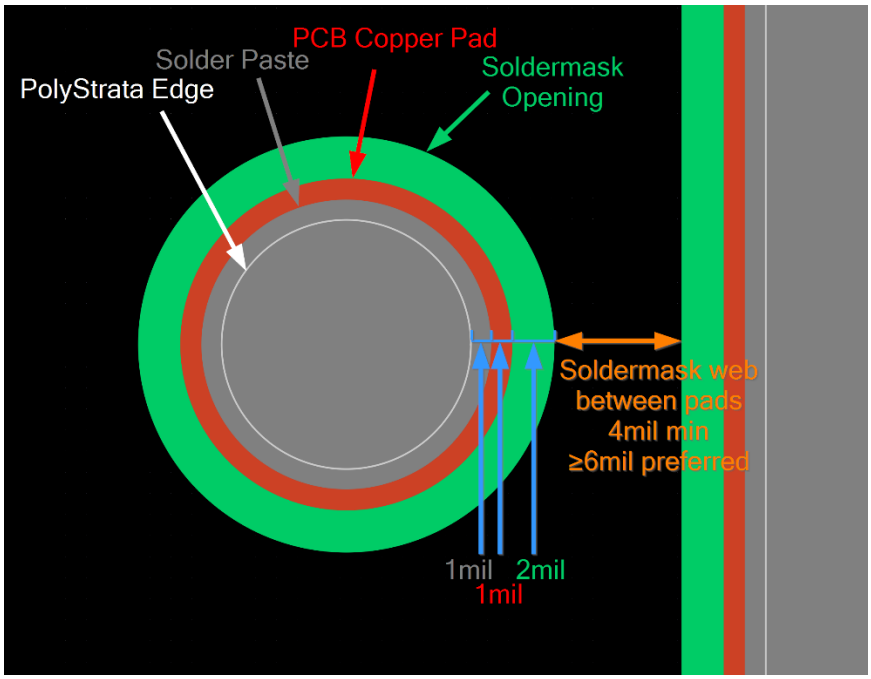


Figure 7 - Footprint Expansion Values

Examples

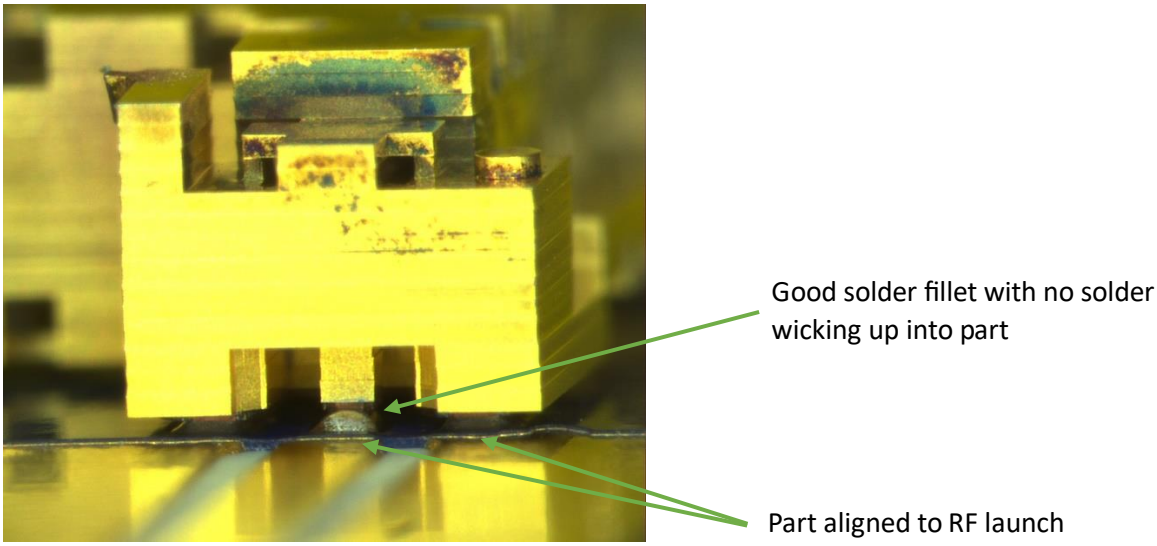


Figure 8 - Good Solder Example

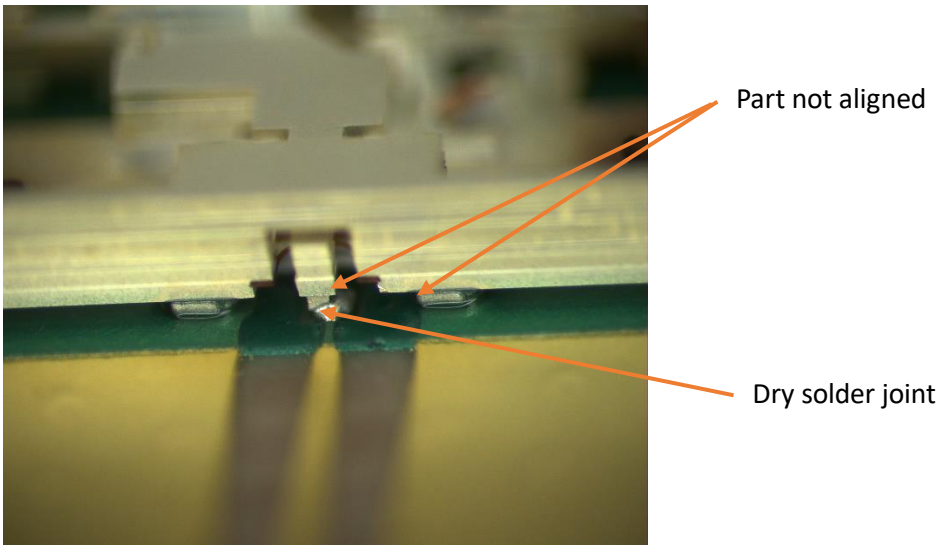
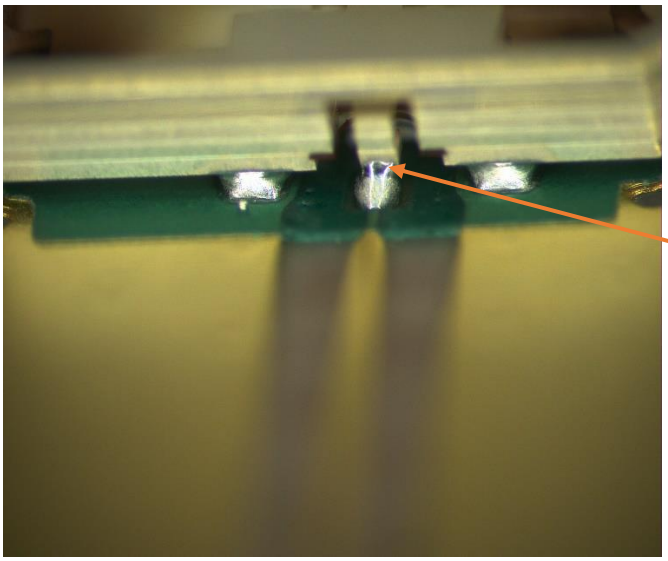


Figure 9 - Alignment Error



Too much solder paste, wicking up center conductor.

Please contact us with any specific questions and we will help guide you towards an effective way to incorporate these devices into your production process.