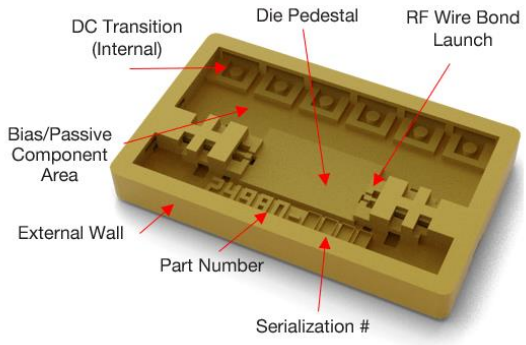
Design and Application Notes for PolyStrata® Die Packages

This document provides general guidelines on how to assemble, handle, and store PolyStrata® Die Packages. The PolyStrata® Die Package is a package substrate product that offers unmatched low-loss and low-parasitic signal handling from MMIC to PCBs and is compatible with a variety of industry standard techniques, as described briefly in this note.

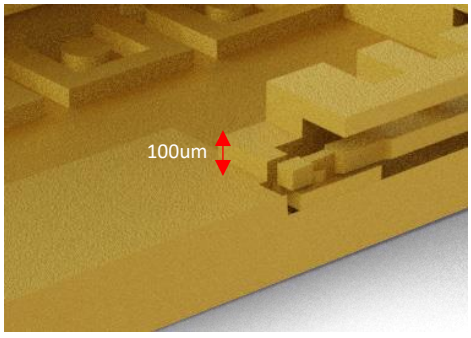
Construction

- The packages are custom-sized based on MMIC dimensions to maximize the substrate area use and optimize RF performance.



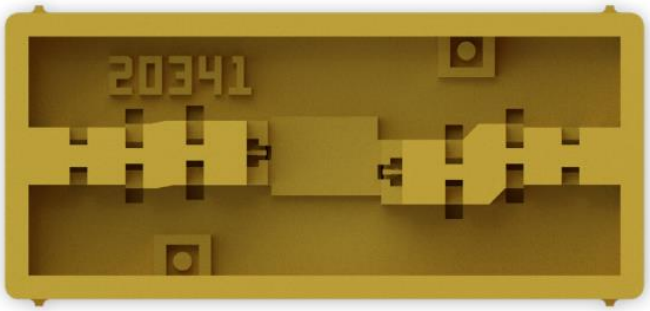
Die Pedestal

- The die pedestal, which is where the die is to be placed on the substrate, is typically designed to be 100 µm larger than the size of the die perimeter.
- To mitigate CTE mismatch to sensitive die, consider the type of die adhesive used or implement a die-on-carrier approach.
- Nuvotronics assumes the die will be attached directly to the pedestal with epoxy or silver sintered paste. The step down from the RF wire bond surface to die pedestal is 100 µm.



Bias/Passive Component Area

- This area is available for adding wire bondable components to be integrated inside the package, depending upon die needs.
- This area can be increased, reduced, and put on both sides of the pedestal to meet die needs. See example:



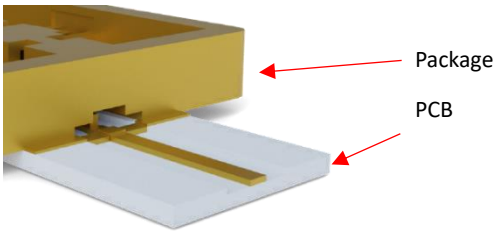
- The typical use case includes size 1515 single layer, wire-bondable 100 pF capacitors in this area to filter gate and drain signals. Any additional components for signal conditioning would be located on the PCB, outside the package.

RF Wire Bond Launch

- Wire bond geometry is critical to achieving the desired performance. See specific substrate datasheet for additional guidance.
- The standard gap between die edge and the transition edge is 50 µm.

RF SMT Transition

The RF package I/Os are designed and tuned with the PCB in mind. Application laminate material and thickness as well as via size and placement must match what is designed. Refer to substrate datasheet and footprint file for correct board geometry.



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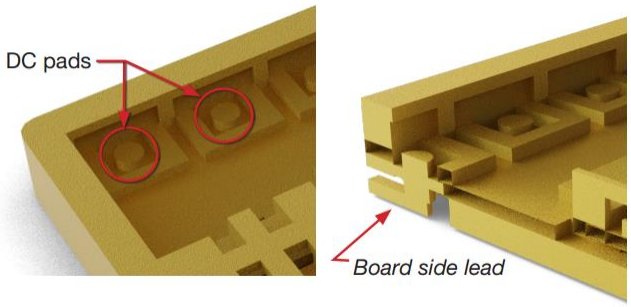
DC SMT Transition

- The DC pins are not as sensitive as RF I/Os.
- Pads internal to the package are 260 µm in diameter and are designed to accept wire bond interconnects.
- These pads feed through to the leads on the bottom of the package.
- The quantity and location of these elements can be modified to meet the needs of the die, including being located on any or all sides of the package.
- The minimum pitch between DC pins is 800 µm with a ground pin in between.

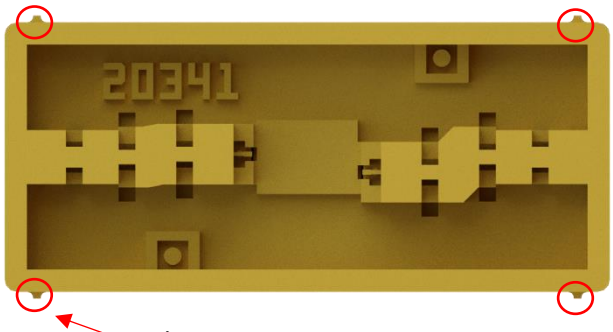


Part Number and Serialization

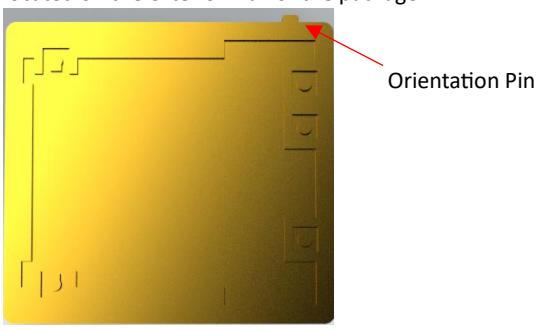
- Each package substrate will contain a part number that identifies the unique design as well as a serialization number that identifies that part's location on the wafer or panel.

Package Walls: Exterior and Interior

- The exterior wall of the package runs around the perimeter of the substrate. Typical wall width is 330 µm to allow for various lid attach methods. The function of this feature is equivalent to the seal ring on LTCC or plastic packages.
- All parts contain a manufacturing feature (tether stubs) that is laser cut prior to delivery. These features are necessary to facilitate batch processing of parts. Discoloration around these features does not affect functionality of the part.

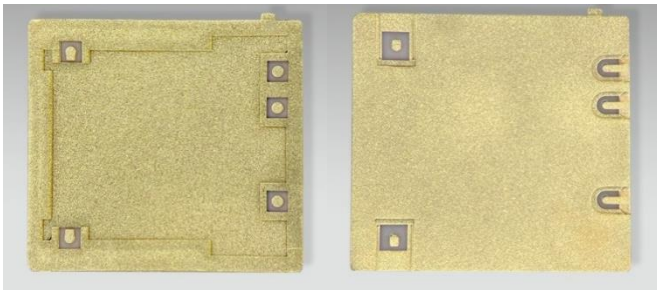


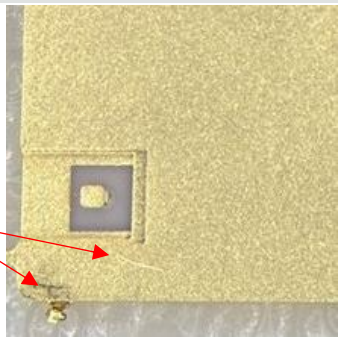
- The geometry of the substrate will vary between different package families. Refer to the datasheet or associate CAD models for specific substrate dimensions.
- Interior walls can be implemented in substrate designs to create channelization and to address cavity resonance issues.
- In addition to the tether stubs, a 150x300 µm orientation pad is located on the exterior wall of the package.



Part Finish

- Wire-bondable direct immersion (minimum 100nm thickness).
  - The DIG process yields a uniform gold finish on part surfaces. Underlying copper shall be completely covered, allowing for a consistent wire-bond or soldering process with little part to part finish variation.





- Proper handling and care should be observed to preserve the gold finish and wire-bondable surface refer to the "Handling and Storage" section for more information.

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Thermal Considerations

- The thermal performance of the package is dominated by the selected die attach approach (epoxy, sintered silver, solder to carrier) and the thermal resistance of the board and thermal management approaches.
- The body of the package is entirely copper, including underneath the die pedestal, maximizing heat spreading and the heat transfer area on the bottom of the package.
- For thermally demanding applications, special attention must be given to the thermal vias in the ground/heat transfer area of the package footprint. This entire area can be used for heat removal, but its effectiveness is determined by PCB design. The effectiveness of the design would depend upon size, space, and type of thermal vias used; for example, copper filled, thickness of substrate, design of thermal planes in the board, or use of embedded copper coin or PCB cutout to allow for direct contact of the heat sink to the bottom of the package.
- A fully detailed CAD model of the package can be provided upon request to assist in thermal analysis.
- When using a copper lid, heat can be removed effectively through the top of the package. However, thermal resistance to the lid is 6.12°C/W.
- The thermal resistance of a 5x5 mm substrate is 2.36°C/W. This is determined through Finite Element Analysis (FEA) from the back side of the die to the bottom surface of the package, including a 25-µm-thick silver sinter die attach interface.
- A fully detailed CAD model of the package can be provided upon request to assist in thermal analysis.
- When using a copper lid, heat can be removed effectively through the top of the package. However, thermal resistance to the lid is 6.12°C/W.

Handling and Storage

Shipping

- Nuvotronics package components are shipped tape and reel.

Handling

- The PolyStrata Die Package design results in the most sensitive RF cavities and surfaces on the interior of the component surrounded by a robust copper ground shell, making these components robust for handling. Scratches or other surface defects on the exterior of the part will not affect part performance.
- Care should be taken to avoid bending/deforming parts. Copper is a ductile material and will deform under excessive force, which may detune interior structures.
- Handling with a vacuum pick tool is recommended.
- Handling with non-marring tweezers is acceptable if care is taken to avoid sensitive features, such as exposed pins on the bottom surface of the substrate.
- Parts should not be placed on fabric, open-celled foam, or stored loose in bags to avoid snags.

Cleaning

- PolyStrata parts are compatible with a wide range of solvents such as isopropyl, acetic acid, hydrofluoric acid, and various flux cleaners.
- Wash temperatures up to 70°C are acceptable.
- Recommend a final isopropanol rinse and dry bake in a nitrogen environment to ensure no remaining chemistry or moisture is internal to part after the cleaning process.
- Special attention to Foreign Object Debris (FOD) concerns described earlier should be made during cleaning. The presence of excessive loose conductive or nonconductive particles (~50 µm–250 µm size), in the solutions or on the devices being cleaned, could result in FOD entering the interior of the PolyStrata part and becoming stuck. This could detune or cause a short in the part.
- A 100% argon plasma cleaning is recommended immediately prior to wire bonding. Do not use oxygen plasma.

Part Storage

Substrates should be stored in compliance with JEDEC JEP160 guidance for devices with sensitivity to oxygen.

Typical Environmental Test Results

Test	Method	Parameters	Result
Moisture Sensitivity	IPC / J-STD-020E, MSL1	168 hrs., 85C/85RH, 3x solder reflow	PASS
Accelerated Life	JESD22-A118B	130°C, 85% RH, 96 hrs.	PASS
Thermal Cycling	JESD22-A104E, Cond. B	-55°C to 125°C, 700 cycles	PASS
Mechanical Shock	JESD22-B104C, Cond. B	1500g, 0.5 ms, 6 orientations, 5 shocks/orientation, 30 shocks total	PASS
Vibration	JESD22-B103B.01, Cond. 1	20G, 20 - 2000 Hz, 4 sweeps/axis, 4 min./sweep	PASS

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Wire Bonding Guidelines

- Substrates are compatible with gold ribbon, wire, and ball bonding processes.
- Parts must be sufficiently secured during bonding on heated stage. Consider part shape and bottom surface geometry when planning securing method.
- Parts will remain wire bondable after multiple thermal excursions through solder reflow (6 min @ 260°C), in ambient environment, with bond strengths above MIL-STD 883 pull test requirements. Cleaning with argon plasma must be conducted prior to bonding.

Lid Attach Options

- The lid should be attached to the external wall using epoxy or solder. Laser sealing and seam sealing may be possible but these methods have not been explored by Nuvotronics.
- Lid material can be metal or plastic. It is important to account for potential cavity modes when considering lid options. The use of an RF absorber may be required to mitigate resonance issues.
- A cavity-style lid will be needed if wire bond loop height is proud of external package walls.

PCB Design

- Refer to specific part datasheet for part-specific information on PCB design needs.
- A recommended layout for each package is available upon request, via DXF format.
- The DXF will contain the following layers:
    - Part Keep Out – Minimum allowable encroachment of neighboring components and board features
    - Vias – Location and size of vias from top to the ground layer of the microstrip
    - Package Footprint – The physical bottom surface of the package that contacts the board
    - Top Copper – Top layer copper pattern
    - Top Paste – Recommended stencil opening
    - Top Mask – Solder mask pattern
- Refer to notes on board thickness and material; these are crucial to achieving specified performance.

If required, thermal vias can be placed anywhere underneath the body of the package, provided they do not interfere with top layer pattern geometry or the vias for the RF transitions. The entire body of the package can be used for heat transfer.

SMT Guidelines

- Placement force should be kept to < 400 grams.
- PolyStrata Die Packages are compatible with all solder reflow profiles described in J-STD-020.

Note: Because the entire substrate body is metal, solder will wick across these surfaces. This does not indicate a failure but should be minimized. Recommend to use of 4mil thick stencil, unless stated otherwise.

Please contact us with any specific questions and we will help guide you towards an effective way to incorporate these devices into your production process.